04/28/05

DAC

Attorney Docket No.: 5649-1135

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Beom-jun Jin
Serial No.: 10/689,981
Filed: October 20, 2003
For: INTEGRATED CIRCUIT DEVICES INCLUDING LOW DIELECTRIC SIDE WALL SPACERS AND METHODS OF FORMING SAME

Group Art Unit: 2815
Examiner: Jesse A. Fenty
Confirmation No. 8976

April 27, 2005

Mail Stop Petitions
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PETITION TO WITHDRAW HOLDING OF ABANDONMENT UNDER 37 C.F.R. § 1.181(a) AND STATEMENT OF SUPPORT

Sir:

Please consider this Petition to Withdraw Holding of Abandonment under 37 C.F.R. § 1.181(a) for the above-referenced application in light of the supporting facts and statements presented below.

(1) The present application was filed on October 20, 2003.

(2) An Office Action was issued by the U.S. Patent and Trademark Office on September 27, 2004.

(3) On October 18, 2004, Applicant filed a Response to Restriction Requirement and return receipt postcard by the United States Postal Service (a copy is attached as Exhibit A). On October 25, 2004, Petitioner received the return receipt postcard bearing an OIPE stamp of October 20, 2004, indicating official receipt of the above-mentioned papers at the U.S. Patent and Trademark Office on October 20, 2004 (a copy is attached as Exhibit B).

(4) On April 4, 2005, a Notice of Abandonment for lack of reply to the Office Action issued, and was received at our office on April 6, 2005.

Petitioner was unaware that a timely reply had not been received by the U.S. Patent and Trademark Office as the return receipt postcard was indicative of timely receipt of response to the September 27, 2004 Office Action Mailed.

Petitioners believe that no fee is due. However, the Commissioner is authorized to charge any deficiency, or credit any overpayment, to Deposit Account No. 50-0220.

Petitioners respectively request that the above-identified application be restored to active status for at least the reasons discussed above.

Respectfully Submitted,

Robert N. Crouse
Registration No. 44,635

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CERTIFICATE OF EXPRESS MAILING UNDER 37 C.F.R. § 1.10

"Express Mail" mailing label number: **EV 674759055 US**
Date of Deposit: **April 27, 2005**
I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to: Mail Stop Petitions, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Audra Wooten

Exhibit A

Attorney Docket No. 5649-1135 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Beom-jun Jin
Serial No.: 10/689,981
Filed: October 20, 2003
For: INTEGRATED CIRCUIT DEVICES INCLUDING LOW DIELECTRIC SIDE WALL SPACERS AND METHODS OF FORMING SAME

Group Art Unit: 2815
Examiner: Jesse A. Fenty
Confirmation No.: 8976

October 18, 2004

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO RESTRICTION REQUIREMENT

Sir:

Applicant provides the present Response to Restriction Requirement to address the issues raised in the Restriction Requirement dated September 27, 2004. Applicant respectfully requests entry of this Response and allowance of the application.

It is not believed that an extension of time and/or additional fee(s), including fees for additional claims, are required, beyond those that may otherwise be provided for in documents accompanying this paper. In the event, however, that an extension of time is necessary to allow consideration of this paper, such an extension is hereby petitioned under 37 C.F.R. §1.136(a). Any additional fees believed to be due in connection with this paper may be charged to our Deposit Account No. 50-0220.

Amendments to the Claims are reflected in the listing of claims, which begin on page 2 of this paper.

Remarks/Arguments begin on page 5 of this paper.

1. (Original) An integrated circuit device comprising:

a conductive contact in a hole in an interlevel dielectric layer;

a first spacer having a first dielectric constant on a side wall of the conductive contact; and

a second spacer having a second dielectric constant that is less than the first dielectric constant located between the first spacer and the side wall of the conductive contact.

2. (Original) An integrated circuit device according to Claim 1 wherein the first spacer comprises silicon nitride and the second spacer comprises silicon oxide.

3. (Original) An integrated circuit device of Claim 1, wherein the thickness of the first spacer is in a range between about 10 Å and about 300 Å.

4. (Original) An integrated circuit device according to Claim 1 wherein the thickness of the second spacer is in a range between about 10 Å and about 200 Å.

5. (Original) An integrated circuit device according to Claim 1 further comprising:

a conductive line in the interlevel dielectric layer adjacent the first spacer opposite the conductive contact.

6. (Original) An integrated circuit device according to Claim 1 further comprising:

a contact pad in a substrate, wherein the conductive plug contacts the contact pad.

7. (Original) An integrated circuit device according to Claim 6 wherein the second spacer extends along the side wall to contact the contact pad; and

wherein the first spacer does not contact the spaced isolated from the contact pad.

8. (Original) An integrated circuit device comprising:

a substrate;

a first interlevel dielectric layer which is formed on the substrate, wherein contact holes are formed in the first interlevel dielectric layer;

first contact spacers which are formed along the side walls of the first interlevel dielectric layer which is exposed via the contact holes, the first contact spacers being formed of silicon oxide;

second contact spacers which are formed of silicon nitride and formed on the first spacer; and

contact plugs which are formed between the second contact spacers.

9. (Original) The integrated circuit device of claim 8, wherein between the substrate and the first interlevel dielectric layer, further comprising:

a second interlevel dielectric layer which is formed on the substrate; and

contact pads which are formed in the second interlevel dielectric layer and electrically connected to the contact plugs.

10. (Original) An integrated circuit device comprising:

an integrated circuit substrate in which source/drain regions are formed;

a first interlevel dielectric layer which is formed on the integrated circuit substrate;

gate line patterns which are formed in the first interlevel dielectric layer;

contact pads which are present between adjacent gate line patterns in the first interlevel dielectric layer and electrically connected to the source/drain regions;

a second interlevel dielectric layer which is formed on the first interlevel dielectric layer, wherein contact holes, through which the contact pads are exposed, are formed in the second interlevel dielectric layer;

first contact spacers which are formed along the side walls of the second interlevel dielectric layer which is exposed via the contact holes, the first contact spacers being formed of silicon oxide;

second contact spacers which are formed of silicon nitride and formed on the first contact spacers; and

contact plugs which are present in the contact holes between the second contact spacers.

11. (Original) The integrated circuit device of claim 10, wherein the second interlevel dielectric layer further comprises:

bit line contact plugs which are electrically connected to some of the contact pads; and

bit line patterns which are formed on the bit line contact plugs and electrically connected to the bit line contact plugs,

wherein the other contact pads, which are not electrically connected to the bit line contact plugs, are exposed through the contact holes.

Claims 12-27 (Canceled).

REMARKS

In response to the restriction requirement of September 27, 2004, Applicants hereby elect Invention I including Claims 1-11 for examination on the merits without traverse. Applicants respectfully request favorable examination of Invention I and allowance of Claims 1-11.

Respectfully submitted,

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Certificate of Mailing under 37 CFR 1.8 (or 1.10)

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on October 18, 2004.

Audra Wooten

Exhibit B

RNC/abw

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Date: 10 - 18 - 04
Doc. No. 5649-1135
Serial No. 10/689,981
Inventor: J.N

Sir: Kindly acknowledge receipt of the accompanying items listed below by placing your receiving stamp hereon and return mailing:

_____ Application Transmittal and:
- ___ Specification pages ____
- ___ No. of Claims _____
- ___ Declaration & POA
- ___ Assignment and Fee
- ___ Small Entity Statement
- ___ Formal Drawings/___ sheets
- ___ Associate Power of Attorney
- ___ Exp. Mail ___ 1st Class Mail
- ___ Other: Response to Rest. Req.

- ___ Check $_____
- ___ IDS & PTO-1449 & ___ refs.
- ___ Amendment & Amend. Transmittal
- ___ Preliminary Amendment
- ___ Issue Fee
- ___ Brief
- ___ Appeal
- ___ Submittal of Priority Doc

OIPE JC32
OCT 20 2004
PATENT & TRADEMARK OFFICE

Respectfully submitted,
MYERS BIGEL SIBLEY & SAJOVEC, P.A.
Attorneys for Applicant